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Towards understanding intrinsic degradation and breakdown mechanisms in SiOCH low-k dielectrics

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The degradation and breakdown mechanisms of a SiOCH low-k material with k = 2.3 (25% porosity) and thicknesses ranging from 90 nm to 20 nm were investigated. By combining the time dependent dielectric breakdown data at positive/negative bias stress with the thickness scaling results, dielectric failure is proven to be intrinsic and not influenced by copper drift or metal barrier deposition induced dielectric damage. It is shown that stress induced leakage current (SILC) can be used as a measure of dielectric degradation. Therefore, low field lifetimes can be safely estimated using SILC extrapolation. Based on our results, both the impact damage model and the power law model have a good accuracy for low field lifetime prediction. Recovery and anneal experiments are used to study the physical nature causing the observed negative flatband voltage shifts in our metal-insulator-semiconductor planar capacitor structures, where hydrogen induced unstable fast and slow donor type interface states are hypothesized to be the root cause of the observed shifts. We suggest that atomic hydrogen is released from the dielectric during electron injection and migrates to the interfacial region. Our model is further supported by an observed irreversible SILC change during the recovery and anneal studies. The degradation mechanism proposed in this work, supported by the low field lifetime data, provides a feasible explanation for intrinsic low-k dielectric failure. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4907686]

I. INTRODUCTION

Continuous development of interconnect architectures towards more advanced technology nodes requires reliable integrated low-k dielectrics. The electrical breakdown strength of dielectric materials is seriously weakened by porosity introduction and spacing reduction, where achieving a fast and accurate evaluation of low-k electrical reliability is extremely important.[1] Time dependent dielectric breakdown (TDDB) is a well-accepted method to estimate dielectric time to failure (TTF) at use conditions. Data collected at high fields are extrapolated to low field use conditions by assuming a given field acceleration lifetime model, where process variability has to be taken into account for advanced nodes.[2,3] In the past years, several models have been proposed and the discussions are still ongoing, especially between the $\sqrt{E}$ model and the impact damage (ID) model.[4–15] Both models[11,12] assume that charges injected in the dielectric have a certain possibility to create intrinsic defects. When the number of defects inside the dielectric reaches a critical value, a conductive path will be formed and lead to a catastrophic breakdown. The relationship between the critical defect number (N_{Critical}) and the charge to breakdown (Q_{BD}) can be written as

$$N_{Critical} = P \cdot Q_{BD} \approx P \cdot (J_0 \cdot Area \cdot TTF), \qquad (1)$$

where P stands for the probability of defect generation, *Area* is the dielectric area, and the initial current density J_0 describes the leakage mechanism. J_0 is assumed to remain reasonably constant during stress. Since in these two models, the same conduction mechanism (Poole-Frenkel emission) is assumed which causes an identical $\sqrt{E}$ term, P plays a key role in the low field TTF extrapolation.[13] The $\sqrt{E}$ model[11] assumes P to be constant, while the ID model[12] proposes a field dependent P. As a result, the $\sqrt{E}$ model (TTF $\sim J_0^{-1}$) gives a more conservative extrapolation than the ID model. Other authors proposed the $\sqrt{E}$ model based on copper driven by electric fields, where a critical number of injected copper ions becomes the breakdown criterion. Suzumura *et al.*[14] suggested a similar relationship as Eq. (1) with a constant P. Chen *et al.*[15] derived a relationship, where TTF $\sim J_0^{-2}$, based on the calculation of copper concentration in the leakage path at a given position and time. In order to draw a safe conclusion on the intrinsic lifetime model, the relationship between TTF and J_0 and the impact of copper on TDDB need to be investigated.

In addition, the nature of defects causing intrinsic degradation in low-k dielectric material is still not well understood. The ID model[13] suggests chemical bond breakage followed by atom movement. The displacement of hydrogen atoms is hypothesized in this model. Miyazaki *et al.*[16] reported that electron impact or randomly stretched Si-O bond generate immobile defects. These defects are suggested to be located symmetrically between two Cu lines in damascene structures. Haase[17] proposed a model to explain the relationship between trap density and current density. In this model, energetic charge carriers are also assumed to create traps but the defect nature is not discussed. The dynamic

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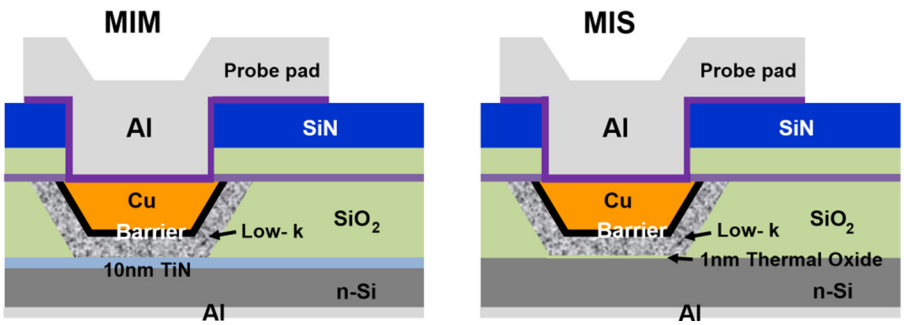

FIG. 1. Cross sections of 100 μm $\times$ 100 μm MIM and MIS planar capacitors.

voltage stressing experiments performed by Lee and Oates[18] showed that the intrinsic damage is independent of the integration process and AC stress frequencies in between 0.01 Hz and 100 kHz, where permanent physical damage in the dielectric is observed. In our work, in addition to standard TDDB measurements, we carried out studies on stress induced leakage current (SILC) and flatband voltage (V_{FB}) shift in order to gain more knowledge about low-k dielectric degradation.

II. EXPERIMENTAL

Dedicated 100 μm $\times$ 100 μm metal-insulator-metal (MIM) and metal-insulator-semiconductor (MIS) planar capacitors[19] are used in this work. Their schematic cross sections are shown in Fig. 1. A SiOCH based low-k dielectric with a porosity of 25% and a dielectric constant of 2.3 is deposited on a 10 nm TiN film in the MIM capacitor and on 1 nm thermal oxide in the MIS capacitor. In the MIM capacitors, the low-k dielectric thickness is ranging from 90 nm to 20 nm. In the MIS capacitors, the low-k dielectric thickness is fixed at 40 nm. Prior to copper seed and plating, different variants of dense low-k protection layers and metal barrier recipes have been applied. The detailed sample list is described in Table I.

III. RESULTS AND DISCUSSION

A. Influence of copper and barrier metal

1. Positive and negative bias TDDB

The MIM capacitor configuration enables to study the role of copper in TDDB by comparing the degradation results under positive and negative bias stress.[20] When applying a negative bias to the top electrode, copper ions cannot drift into the porous dielectric and only intrinsic dielectric degradation is possible. On the other hand, when applying a positive bias to the top electrode, copper ions can potentially drift into the dielectric. Our experiments demonstrate the same degradation behavior at different polarities, as shown in both the *J-t* curve plots and the lifetime Weibull plot (Fig. 2). These results suggest that intrinsic dielectric degradation under positive bias stress is dominant and the leakage current increase observed in the final phase of degradation is not caused by the accumulation of copper ions.

TABLE I. The detailed sample list.

Split		Low-k thickness	Protection layer + Metal barrier
S1	MIM	90 nm	N. A.
S2	MIM	60 nm	PVD TaN/Ta
S3	MIS	40 nm	PVD TaN/Ta
S4	MIM	40 nm	PVD TaN/Ta
S5	MIM	40 nm	12 nm non-porous low-k + ALD TiN + PVD TaN/Ta
S6	MIM	20 nm	12 nm non-porous low-k + ALD TiN + PVD TaN/Ta

2. Dielectric thickness scaling

TDDB and constant current TDDB measurements are performed on low-k films with different thicknesses. For SiOCH low-k dielectric films with a protective layer, using constant current TDDB avoids incorrect field determination caused by the heterogeneous stack. A clear dependence of TTF on J_0 is observed in Fig. 3. For a given stress condition (with the same J_0), similar TTFs strongly suggest that film degradation is insensitive to film thickness in the range of 20 nm–90 nm.[8] In addition, since the non-porous protection layer reduces dielectric damage by barrier deposition and metal driven in by electrical stress, the same reliability performance of low-k dielectrics with and without the protection layer suggests an intrinsic degradation mechanism during TDDB.

B. SILC and conduction mechanism

The SILC behavior was studied using S4. A voltage ramp (VR) test is repeated during the TDDB measurement. Fig. 4(a) shows the VR test results collected both on a stressed film and non-stressed film. The increase of low field leakage currents under positive and negative bias VR is similar. These results suggest that SILC is caused by a symmetric degradation inside the dielectric between the two metal electrodes.[16] Besides the steady SILC, a transient current component is also observed in Fig. 4(b). In theory, this transient current could be caused by a charging process at the interface. However, Fig. 4(b) reveals that the steady SILC is not influenced by this transient current component. Lee and Oates[18] also reported that this charging/discharging process does not affect dielectric failure. As a result, we focus on steady SILC.

Fig. 4(a) suggests that the increase rate of SILC at low fields is higher than at high fields. The β extracted from $\ln(J/E) \sim \beta/kT \cdot \sqrt{E}$, as based on Poole-Frenkel (PF) emission theory,[21] quantifies the *J-E* slope below 4.0 MV/cm. The

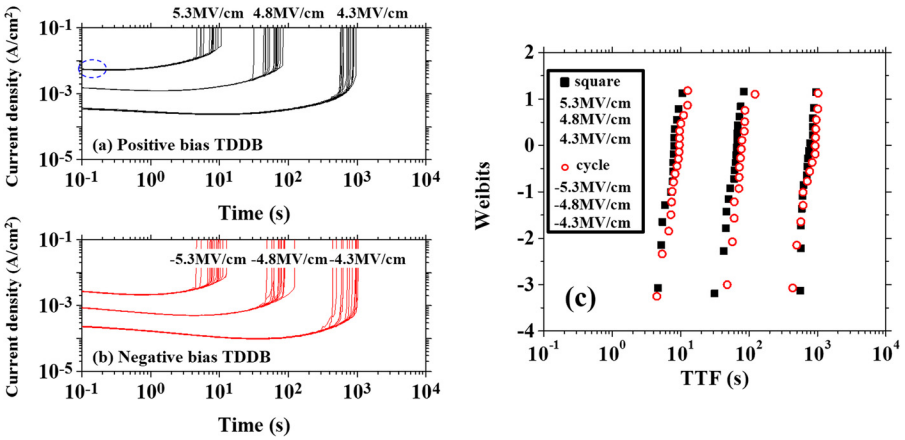

FIG. 2. Positive (a) and negative (b) bias TDDB results at 100 °C (c) Weibull plot of the data obtained using positive and negative bias TDDB (S4).

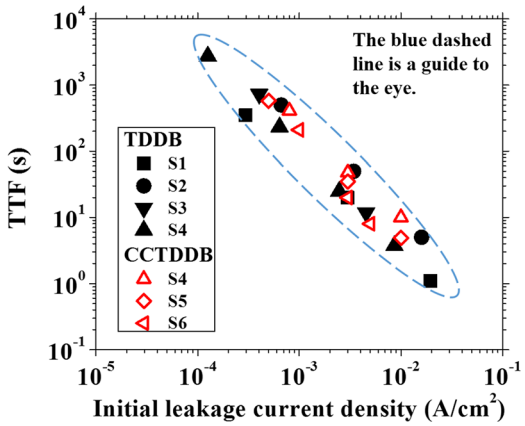

FIG. 3. Constant voltage TDDB and constant current TDDB (CCTDDB) measurements (positive bias stress) of different films at 100 °C: relationship between initial leakage current density and TTF.

relation between β and t_{stress} at different stress conditions is plotted in Fig. 4(c). In the field range below 4.0 MV/cm, the PF emission is the dominant conduction mechanism, as the value of β_0 is in good agreement with its theoretical value

$$\beta_0 = \sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_r}}, \tag{2}$$

where q is the elementary charge, ε_0 is the vacuum permittivity, and ε_r is the high frequency dielectric constant. However, prior to breakdown β gradually decreases to half of its initial value which suggests that donor type trap generation is the cause of SILC.[22] During electrical stress, the relative contribution of acceptor states decreases compared to those of free electrons and donor type defects. As a result, the compensation factor ξ in the extended PF model[23] is shifting from 1 to 2, leading to a decreased β

$$\beta = \frac{\beta_0}{\xi}. \tag{3}$$

This decrease has been often reported for porous low-k dielectrics[22,24,25] and hydrogenated amorphous silicon alloys.[26,27] The lower rate of current increase at fields above 4.5 MV/cm is commonly explained by enhanced electron trapping in low-k dielectrics due to small ramp rates used during VR test.[17,28] However, for the low-k material characterized in this work, the initial current density value measured at +5.3 MV/cm in Fig. 2(a) is the same as the one measured during the VR test. This suggests that the VR test is not affected by the applied ramp rate and is able to represent the initial state of leakage current. In addition, β

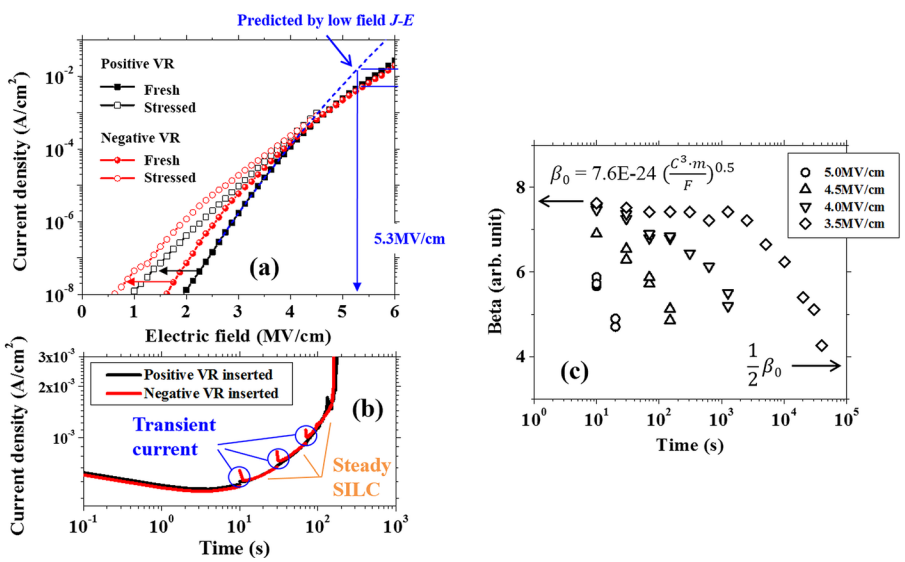

FIG. 4. (a) Positively and negatively biased VR test results obtained on a non-stressed film and a film stressed at 4.5 MV/cm for 150 s at 100 °C. (b) *I-t* curves during 4.5 MV/cm stress with positive and negative VR inserted. (c) Dependence of β on t_{stress} at four different constant field stress conditions (S4).

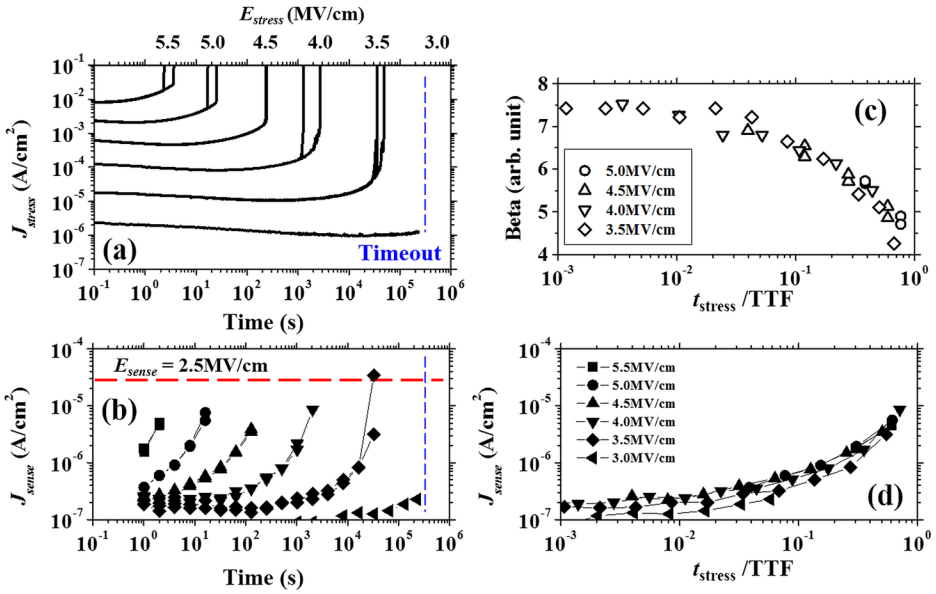

FIG. 5. A sense stress at 2.5 MV/cm is added during the TDDB tests at higher fields at 100 °C: (a) relationship between J_{stress} and t_{stress}, (b) relationship between J_{sense} and t_{stress}, (c) relationship between β and t_{stress}/TTF, (d) relationship between J_{sense} and t_{stress}/TTF (S4).

calculated from this field region is equal to half of the low field β_0. This phenomenon is then explained by the onset saturation of PF emission due to the conductivity change.[29]

C. TDDB lifetime model

1. TTF extraction by using SILC measurements

In order to have a better monitoring of SILC, a sense stress at 2.5 MV/cm is added during the TDDB measurements performed at higher fields ranging from 3.0 to 5.5 MV/cm, where at each sense point, the current density J_{sense} is measured. J_{sense} vs. t_{stress} is then plotted together with J_{stress} vs. t_{stress} in Figs. 5(a) and 5(b). When the sense current reaches a certain critical value, a hard breakdown happens. The J_{sense} increase scales with t_{stress}/TTF, as shown in Fig. 5(d). Using SILC, the same lifetime is extracted as the standard TDDB measurements (sample 4 in Fig. 3), which further proves that SILC can be used as a measure of dielectric degradation.

Our data suggest a direct link between the generated defects and SILC. The critical defect number causing breakdown corresponds to a critical current value. It has been suggested that β changes are proportional to the change in defect number (N)[27]

$$\frac{\beta}{\beta_0} \approx 1 - K \cdot N, \tag{4}$$

where K is a constant. Therefore, Fig. 5(c) again shows that the generated defects mainly depend on t_{stress}/TTF.

2. Package level (PL) TDDB

PL TDDB measurements are performed to further verify TTFs extracted by fitting SILC. A Weibull plot containing both wafer level (WL) and package level results is shown in Fig. 6. From this plot, it is found that the Weibull slope is not sensitive to the electric field. The $t_{63.2\%}$ extracted at 3.5 MV/cm and 3.0 MV/cm by fitting SILC shows a very similar value compared to the TTF extracted by PL TDDB measurements, as shown in Figs. 7(a) and 7(b).

In Fig. 7(a), the dependence of the WL and PL TDDB lifetime on J_0 is fitted by a relationship of TTF $\sim J_0^{-1.57}$, which is in good agreement with the literature.[8,10] The exponent of -1.57 strongly suggests that both the electric field and the leakage current influence lifetime extrapolation. As a result, for the intrinsic dielectric degradation characterization, the $\sqrt{E}$ model[11] which assumes a constant P is too conservative (TTF $\sim J_0^{-1}$). This exponent of -1.57 also excludes the other two $\sqrt{E}$ models assuming copper diffusion,[14,15] where a J_0^{-1}- and J_0^{-2}-dependence on TTF is expected, respectively. Note that, as $\ln(J_0)$ is a function of $\sqrt{E}$, the $\sqrt{E}$ model could still provide a good empirical fit by using field dependent acceleration factors which include the E-J_0 behavior change at different fields. For reasons mentioned above, the physics behind such fit is however lacking.

For a relevant reliability modeling assessment, we only focus on the TTF and E relation from TDDB measurements in the low field region ($E \leq 4.0$ MV/cm). Our data support the ID model,[12] where the TTF is described as

$$TTF \sim \frac{C}{E} \cdot \exp\left(-A\sqrt{E} + \frac{B}{E}\right), \tag{5}$$

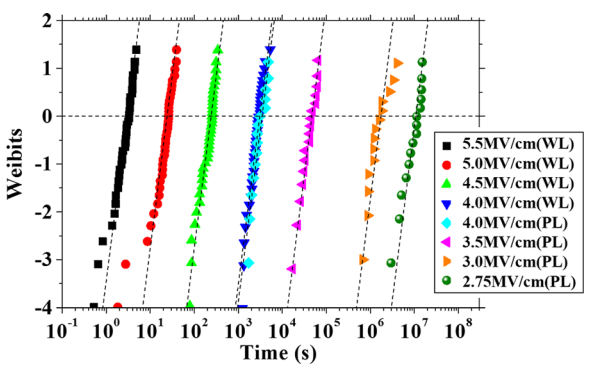

FIG. 6. Weibull plot of the data obtained using WL and PL TDDB measurements at 100 °C (S4).

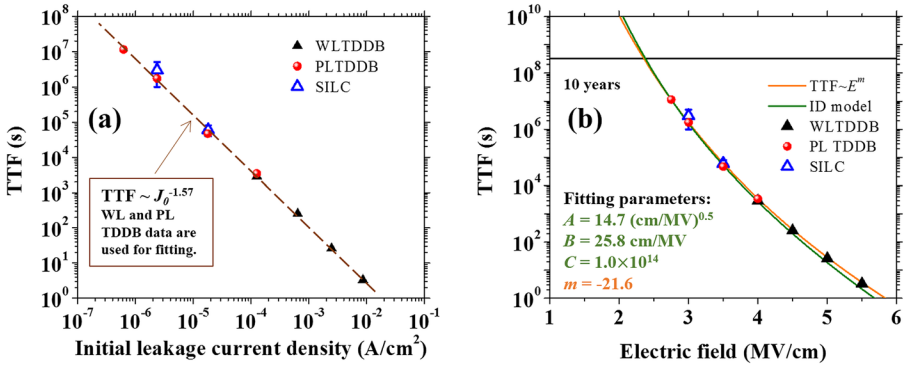

FIG. 7. Lifetime extrapolations including the WL and PL TDDB results and the low field data extrapolated by using SILC at 100 °C: (a) relationship between TTF and J_0, (b) relationship between TTF and E (S4).

where A, B, and C are fitting parameters. A can be calculated from data shown in Fig. 4(a) by using the relation of $\ln(J_0/E) \sim A\sqrt{E}$ ($E \leq 4.0$ MV/cm) and B is extracted from $\ln(\mathrm{TTF}\cdot J_0) \sim B/E$. Hence, C is the only parameter to be fitted in the equation.[10] As shown in Fig. 7(b), using the ID model, a good fit of the TTF data is achieved at low fields. The deviation at high fields is explained by the conduction mechanism change shown in Fig. 4(a). Chen and Shinosky[30] argued that for the ID model, an improved lifetime should be observed at a smaller spacing under the same field. However, as discussed in Refs. 12 and 13, the critical thickness causing this phenomenon is less than 5 nm. Therefore, the theory of ID model is not contradictive to the results discussed so far. In addition, it is found that a power law relation (TTF $\sim E^m$)[31] with m value of −21.6 shows a very similar trend compared to the ID model in the low field region and can reproduce the relation between TTF and E above 4.0 MV/cm.

D. Voltage shift in *C-V* curve

Both the ID model and the power law model explain our low field SILC and TDDB data well. In order to gain further insight, we used our MIS test vehicle to study defect properties in the dielectric during TDDB and during recovery and anneal experiments where the V_{FB} shift is used as a standard measure for trapped charges.[21]

1. V_{FB} shift

We used n-type MIS capacitors integrated with a 40 nm low-k dielectric (S3) to monitor the V_{FB} shift during constant voltage stress. The bias during C-V measurement at 10 kHz is always applied to the top metal electrode.

As shown in Fig. 8, a negative V_{FB} shift is observed for all stress levels, which implies accumulation of positive charges in the system during stress. For low-k dielectrics, this positive charge accumulation is often related to copper diffusion processes.[32] However, the data from Ciofi *et al.*[33] show no V_{FB} shift after copper injection into a thermal oxide suggesting that these two phenomena are not always linked to each other. Our results, where a similar TDDB performance between S3 and S4 is observed as shown in Subsection III A 2 (Fig. 3), as well indicate that the accumulated positive charges are not caused by copper diffusion. Moreover, if copper ions or positive charge accumulation at the anode are the reason for the observed V_{FB} shift, the field enhanced leakage current should be orders of magnitude higher than the value observed in Fig. 9(a). For example, based on the J-E characteristic (not shown) a V_{FB} shift of only −2 V is required to explain the indicated current increase. Also the accumulated positive charges can be regarded by directly calculating the enhanced cathode field E_{Si} by using[34]

$$E_{si} = E_{appl} + \frac{\Delta V_{FB}}{Thickenss_{low-k}}. \quad (6)$$

If the positive charges were located in the low-k dielectric, E_{Si} after 128 s stress should have already exceeded the low-k dielectric intrinsic E_{BD} a result, it is proposed that interface states generated within the 1 nm thermal oxide (Fig. 1) explain the observed V_{FB} shifts. The entire C-V curves during 4.8 MV/cm stress at 25 °C are shown in Fig. 9(b). The curves are stretched-out and show an hysteresis, indicating the generation of both fast and slow interface states.[35]

2. V_{FB} recovery and anneal

To further investigate the above mentioned interface states, we study their recovery and annealing behavior. After a high field stress, two capacitors from S3 are stored at two lower field conditions while the third one is stored under at 0 MV/cm, where the V_{FB} shift during storage is shown in Fig. 10(a). The V_{FB} is shifting back towards to its original value, suggesting a decrease in the number of positive charges. This decrease can be interpreted as electron charging in bulk traps or physical removal of unstable interfacial states. A complete V_{FB} recovery would take more than 10 years,

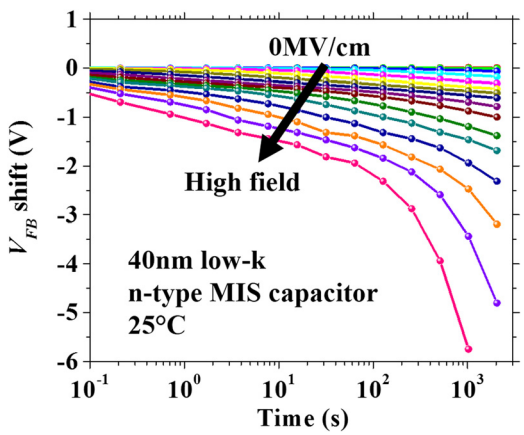

FIG. 8. V_{FB} shift during constant voltage stress at 25 °C (S3).

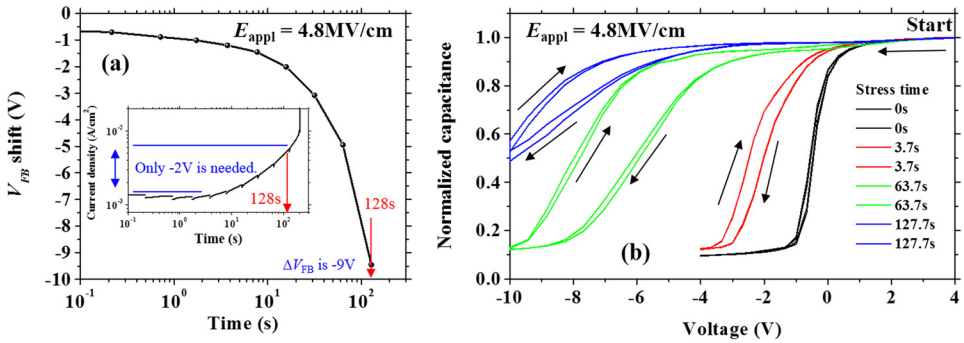

FIG. 9. (a) *I-t* and V_{FB} shift during 4.8 MV/cm stress at 25 °C. (b) Entire *C-V* curves of two samples during 4.8 MV/cm stress at 25 °C (S3).

where this long time scale does not fit the reported theory of electron charging since the charging process normally takes less than 1000 s predicted by the tunneling front model.[36] The samples recovered under the two low field conditions show exactly the same recovery behavior as the 0 MV/cm case. These results are also not in agreement with the electron charging theory.[37] Thus, we believe the recovery kinetics including the physical removal of the charged centers at the interface.

As shown in Fig. 10(b), by comparing the entire *C-V* curves on stressed samples before and after the storage for 2048 s at 0 V, a recovery already happens at room temperature corresponding to a decreased number of fast interface states. Another stressed MIS capacitor annealed at 200 °C for 1200 s in an oven further reveals the unstable nature of fast and slow states. The *C-V* curve is much less stretched-out and its hysteresis is close to that of the fresh sample. V_{FB} also recovers much faster at this elevated temperature.

From the study of V_{FB} recovery and anneal, it is clear that the fast and slow interface states observed in this work show a very similar nature with the reported hydrogen induced interface states.[35,38,39] It is reported that during stress, atomic hydrogen is released from the oxide or the SiO_2/metal interface due to electron injection. The presence of atomic hydrogen at the Si/SiO_2 interface generates these interface states. These interface states are positively charged when the Fermi level is at midgap and contribute to a negative V_{FB} shift causing the so called "turn around effect." During storage, these interface states are already unstable at room temperature following log(time) annealing kinetics whereas they are rapidly removed by a short annealing at temperature above 150 °C. Therefore, the electrical stress of the low-k dielectric discussed here appears to involve the same generation and migration of atomic hydrogen, which is consistent with the speculation of the ID model and the power law model.

E. SILC recovery and anneal

The recovery and anneal tests also help to gain insight in the nature of the donor type defects in the bulk dielectric material. For this, the behavior of SILC in the MIM capacitors with a 40 nm low-k dielectric (S4) is studied. In Fig. 11, three low electric fields are applied after a high field stress and the SILC is monitored at different fields. As already discussed in Sec. III B, the steady SILC on stressed capacitors is independent of charging and discharging. Still we observed a slow recovery of the SILC at room temperature. This recovery of stressed low-k dielectrics has been also reported by other authors,[18,28] where the detailed mechanism of this behavior is not clear. Our results, where the same rate of SILC decrease is observed when applying different low fields in the second step, indicate that the recovery is related to the physical removal of donor type defects in the bulk. Charging/discharging is unlikely to happen due to the slow recovery and the field independent behavior. These observations are similar to those of the V_{FB} shifts discussed above.

The generated donor type defects in the dielectric are unstable, as a short high temperature anneal induces full recovery. As shown in Fig. 12(a), three samples are subjected to a constant voltage stress at 25 °C, 100 °C, and 175 °C, respectively. In order to achieve the same amount of SILC increase representing a similar level of degradation, the stress fields are adjusted for each temperature. After high field stress, the samples are stored and sensed at 2.5 MV/cm for 2000 s to monitor SILC. The recovery of SILC is described by

$$\text{SILC recovery ratio} = \frac{\log[J(t)] - \log\left(J_{Baseline@2.5MV/cm}\right)}{\log(J_0) - \log\left(J_{Baseline@2.5MV/cm}\right)}, \tag{7}$$

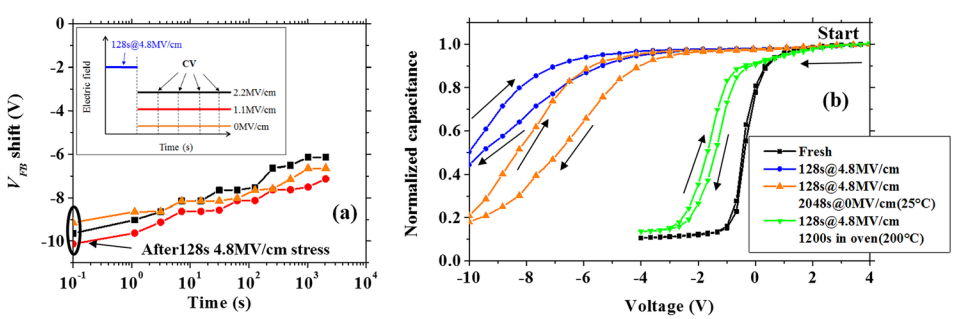

FIG. 10. (a) V_{FB} shift versus recovery time with three different fields applied during storage at 25 °C. (b) *C–V* curves of a fresh sample, a sample stressed for 128 s at 4.8 MV/cm, a stressed sample stored for 2048 s at 25 °C at 0 MV/cm and a stressed sample stored for 1200 s at 200 °C in an oven (S3).

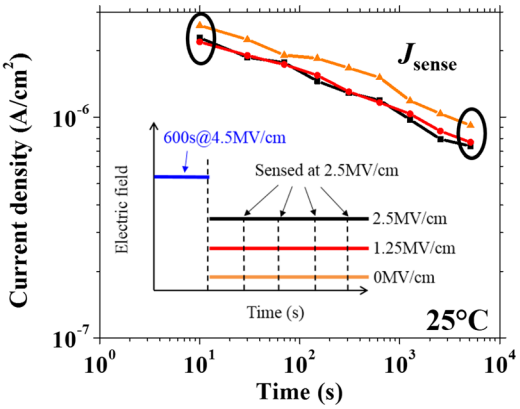

FIG. 11. Three low voltages are applied after high field stress and a fixed sense voltage is used to monitor SILC (S4). The initial leakage current density of a fresh sample sensed at 2.5 MV/cm is smaller than 10^{-7}A/cm^2.

where J_0 is the first sense point (within 0.1 s) after high field stress, $J(t)$ is the leakage current density value at 2.5 MV/cm at storage time t, and $J_{\text{Baseline@2.5 MV/cm}}$ is the initial leakage current density of a fresh sample sensed at 2.5 MV/cm. The results are plotted in Fig. 12(b). The time needed for full SILC recovery (t_{recovery}) can be extrapolated by fitting the data with a semi logarithmic relation (SILC recovery ratio $= a \cdot \ln(t) + b$). It is clear that a high temperature accelerates the process of physical removal of donor type defects in the bulk dielectric.

To check whether the recovery in Fig. 12(b) is a reversible process, we applied a three step measurement which consists of a constant voltage stress at high field at 100 °C, an annealing at 200 °C for three days in the oven, and finally a second stress at the same field and temperature as in the first step. The sum of the initial stress time and the failure time in the second stress step is compared with the lifetime of the samples without the annealing step. The results are summarized in Table II. All $t_{63.2\%}$-percentiles are the same within the experimental error. Our data suggest an irreversible defect/damage generation mechanism which is similar to the findings of Lee and Oates.[18]

TABLE II. $t_{63.2\%}$-percentiles for the different experiments (S4).

No.	Stress condition	$t_{63.2\%}$
1	4.5 MV/cm stress till breakdown	293.3 s (254.9 s–350.2 s)
2	100 s 4.5 MV/cm stress + 200 °C anneal + 4.5 MV/cm stress till breakdown	329.7 s (285.2 s–396.7 s)
3	−4.5 MV/cm stress till breakdown	305.2 s (267.4 s–359.7 s)
4	100 s −4.5 MV/cm stress + 200 °C anneal + −4.5 MV/cm stress till breakdown	275.6 s (238.4 s–331.7 s)

The detailed link between the *I-t* behavior and V_{FB} shifts during the different stress phases is studied by stressing a fresh MIS capacitor (S3-F) and a MIS capacitor that already received first stress step and anneal (S3-SA). The results are shown in Fig. 13. The faster leakage current increase of S3-SA suggests that the dielectric film is not fully recovered. However, at the same SILC level, the V_{FB} shift of S3-SA is much smaller compared to S3-F. If the V_{FB} shift is considered to be caused by the release and migration of atomic hydrogen to the Si/SiO$_2$ interface, the observation of an irreversible defect generation mechanism (faster leakage current increase) and the generation of less donor type interface states (smaller V_{FB} shift) can be explained by the formation of weak metastable bonds during the anneal step and fast breakage of such recovered bonds without releasing atomic hydrogen during the second stress step. Street[40] reported a similar degradation scheme related to hydrogen atom movements in a-Si:H material. During illumination, high defect densities are generated due to the loss of hydrogen from Si-H or hydrogen trapping at deep bond interstitials. Full removal of active defects can be achieved when annealing at temperatures above 150 °C which allows hydrogen to reach

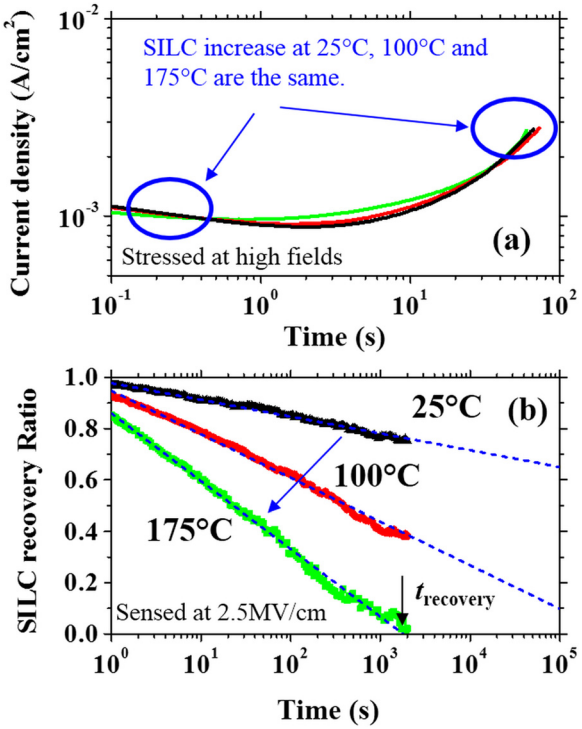

FIG. 12. (a) Current density versus time during constant voltage stress at high fields and at 25 °C, 100 °C, and 175 °C. (b) SILC recovery ratio versus recovery time (S4).

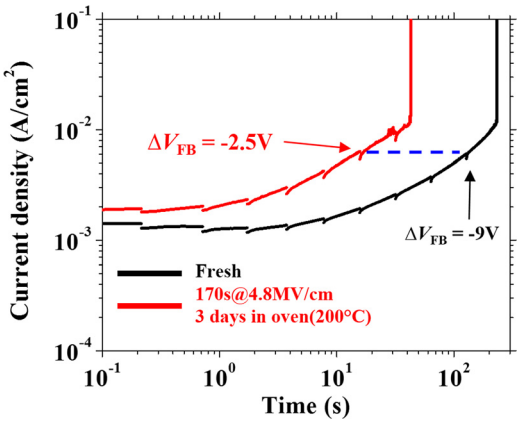

FIG. 13. *I-t* and V_{FB} shift results at 4.8 MV/cm at 25 °C of a fresh MIS capacitor (S3-F) and a MIS capacitor that already received first stress step and anneal (S3-SA).

the previous equilibration. Irreversible changes happen when there is a large scale movement of hydrogen in the system since it maximizes the recreation of weak Si-Si bonds during anneal. In summary, based on the study of SILC recovery during anneal, the generation and migration of atomic hydrogen are again hypothesized to be involved in the low-k dielectric degradation, where bulk dielectric damage is shown to be the source of such released hydrogen atoms.

Note that the mechanism of how hydrogen atoms are generated is not clear at the moment, as both the ID model (focusing on the possibility of injected electron gaining enough energy) and the power law model (discussing the excitation of Si-H bond vibrational modes) provide an explanation and allow accurate low field lifetime predictions. Therefore, in order to achieve more fundamental understanding, additional research efforts are still needed in future.

IV. CONCLUSION

We provide a comprehensive understanding of low-k dielectric degradation. Similar failure times during positive/negative bias TDDB and the independence of TDDB lifetimes on dielectric thickness prove that copper and barrier metals are not influencing low-k dielectric breakdown. We found that low field SILC caused by the generation of donor type traps well describes dielectric degradation, which suggests a direct link between the generated defects and SILC. Our low field TDDB data based on SILC extraction and package level TDDB suggest that the $\sqrt{E}$ model cannot predict the intrinsic degradation as electrical fields are an acceleration factor in the failure process. Instead, the ID model and the power law model give an accurate prediction of low field lifetimes. V_{FB} shift results suggest that both fast and slow donor type interface states are generated during electrical stress. Their unstable nature at room/high temperature indicates the presence of atomic hydrogen at the Si/SiO_2 interface. We propose that this atomic hydrogen is released from the low-k dielectric during electron injection. The study of SILC recovery and anneal further links atomic hydrogen release with low-k dielectric degradation. This degradation process involving hydrogen release and migration is also consistent with the speculation proposed in both the ID model and the power law model.

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